International Journal of Scientific & Engineering Research, Volume 6, Issue 12, December-2015
ISSN 2229-5518

ASSESSMENT OF VLSI FFT FRAMEWORKS DIFFERENCE IN FLEXIBILITY, RAPIDITY, COMPLEXITY AND PROTOTYPING THE FRAMEWORKS FOR SOC TELECOM APPLICATION

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***Abstract*— This paper explains prototyping the integrated circuit of Fast Fourier Transform (FFT) for system-on-chip (SOC) telecommunication. There are three types of assessment of FFT frameworks proposed in wired or wireless OFDM standers in MIMO standers. The three type of framework are, 1. Fully parallel, 2. Pipelined cascade 3. In-place variable-size architecture, these frameworks have different trade-offs, like flexibility, rapidity, complexity and prototyping. The implementation of silicon and assessment with state-of-art prove the works for target application by output from each macro cell. For the throughput requirements up to several Samples/s enabling Ultra-wideband (UWB) communications by using all channels foreseen in the standard the fully parallel is optimized. The pipelined cascade macro cell minimizes complexity for large size. FFTs sustaining throughput up to 100 Samples/s .The in-place variable-size FFT framework macro cell popular for its flexibility by allowing run-time reconfigurability required in OFDMA schemes while attaining the required throughput to support MIMO communications.**

Keywords **–** VLSI frameworks, OFDM communication, FFT.

I. INTRODUCTION

FFT/IFFT frameworks are more important framework for baseband processing in telecommunication. In baseband processing application the design of FFT framework with good throughput and consuming low power have high complexity? This paper proposes three different FFT/IFFT frameworks in VLSI with different trade-off for the telecom application. The main considering part is optimized FPGA implementation in design aspects. We easily reconfigurable at run time and complication time and, so the FPGA framework supports different wireless standards. The main plus of FPGA is providing the prototyping platform to user product, from fixed to mobile terminal and also available in market in low cost.

The advanced OFDM standards for telecom application have a wide configurable space to be faced specification by FFT. The throughput varies from few M samples/s in xDSL (Digital Subscriber Line) modems for residential Internet connections up to G Samples/s in UWB terminals for short-range communication of multimedia contents. In VDSL/BPL application the input-output data width varies up to 16-bits and in UWB it is varies from 4 to 5 bits. In WLAN (wireless local area network) the size of the FFT varies from 64 complex points. Moreover, the FFT engine should be as a parametric IP (Intellectual Property) macro cell and, it should be still configurable at run time to support standards with multi-mode adaptive behavior, if it integrated. We propose different framework approaches with respect to the parallelism, memory access technique and machine arithmetic approaches. Based on these approaches we can analyze the advantage and disadvantage of the three frameworks for FPGA technology.

This paper explains the FFT processing core for OFDM communication standards, suitable FFT framework for high throughput application and cascade configuration of FFT which reduce the complexity and increase the performance in large size FFT application. And optimize the run time reconfigurable still which supporting the high throughput application by in-place variable-length FFT core with parallel butterfly processor. For increasing the WiMAX terminals for run-time FFT size configuration and throughput up to M samples/s to support MIMO (multi input multi output) communication, these frameworks are very suitable. Finally we can compare the FFT VLSI frame work prototyping for OFDM telecom application and producing the best one for the target application.

II. COMMUNICATION STANDARDS OF OFDM:

MIMO-OFDM framework: OFDM standards encourage the development of wired and wireless communication standards such as digital broadcasting of audio and video information in terrestrial and handheld systems, WLAN for medium range indoor networking, UWB radio for high data rate personal area network.

In single carrier modulation OFDM based system provide a maximum strength for reducing the cross-talk, channel fading, and distortion in multi path. The channel equalization is reduced in OFDM channels, because of the transmitted data spread over the orthogonal sub carriers. So the OFDM system is more suitable for the narrow band application rather than the rapidly modulated wide band application. In IEE standard 802.16e the OFDM move as a multi carrier access technique (OFDMA), where the carrier signal is clustered in too many subsets and dynamically assign to each user, so the channel capacity is shared by

multiple users. The FFT uses the similar baseband processing. The FFT uses multi-carrier symbol modulation in receiver side and the IFFT uses the same multi-carrier symbol modulation in transmitter side.

In modulation of IFFT the cycle extension of the symbol is taking place of to insert the guard band for time interval to handle the time-spreading and eliminate the inter symbol interference. If the communication is based on the time division duplexing the FFT and IFFT operation is merged in single processor, so the transceiver worked either as a receiver mode that is demodulated by the FFT .as a transmitter mode menace that demodulated by IFFT .it is in half duplex mode. In full duplex mode the communication is based on frequency division duplexing mode. The OFDM connected with MIMO technique for increasing the system capacity and diversity gain. The IEE standards 802.16 WMAN and 802.11n WLAN is used the MIMO technique. These techniques used multiple antennas for both receiver and transmitter side to make full use of spatial diversity and spatial multiplexing. It increase the capacity of MIMO link by simultaneous transmitting from each transmitting antenna .it transmit the independent data stream in the same time slot and frequency band. At the receiver side the multiple data streams are differentiated by channel information about the propagation path. The data streams are propagated parallel from different antenna, so the throughput is linearly increased by adding of antenna.

The spatial diversity increases the diversity order of MIMO link to reduce the fading by code the signal across the time and space using special space-time code technique that is Alamouti code. At the receiver side, to achieving the diversity gain, the multiple replicas of the signal is combined.

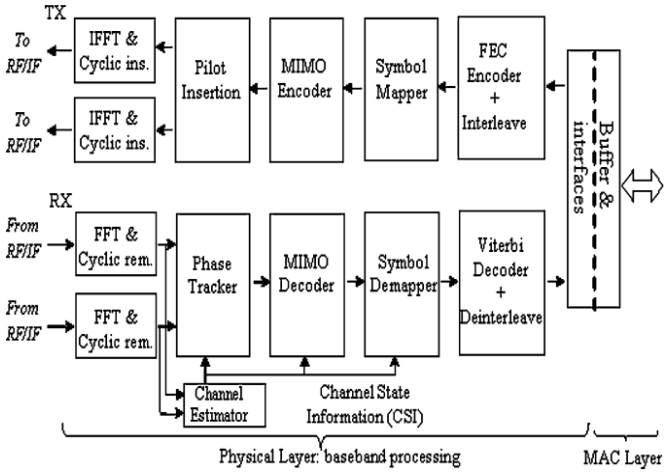

Fig. 1 WLAN 2×2 MIMO-OFDM scheme

The above figure 1 explains the base band processing framework of the 2x2 WLAN MIMO-OFDM systems with two transmitter and receiver path. Based on the transmitter receiver path the FFT and IFFT processors are integrated in a transceiver. In an M×M OFDM-MIMO system, up to M different streams can be transmitted concurrently over multiple antennas; to serve these streams, M FFT and M IFFT processing units working in parallel are required, thus increasing area by a factor M. Alternatively, a lower number of P processors, with P ∈ [1 M], can be used in a time-division way, but to sustain the same data throughput, the clock frequency of the P processors should be increased by a factor M/P.

A. Processing of MIMO-OFDM:

The different OFDM standards are characterized by different terms of FFT/IFFT requirements, in terms of I/O data width varied from 4-16 bits, 64-8192 points of transform length, 1M samples/s to several G samples/s of throughput. The FFT/IFFT requirements for the processing are shown below table 1 and figure2. The requirement range is between two extremes: that is small size FFT with high throughput application for example, the UWB, required large size FFT but low throughput. Some standards carry multiple modes that requires different configuration in terms of FFT length, throughput for protect the various problems for connecting the user, channel condition, bandwidth of the communication, and latency. Here we propose the macro cell have been designed for reuse approach and the FFT length and I/O bits width.

standard	FFT size	I/O data width (bits)	Throughput M samples/s
DVB-T/H	2048-8190	8	10
DAB	256-2046	9	8.2
VDSl	256-4094	16	1-32
802.11a	62	8	20
802.16d/e	128-2048	10	1.2-20
802.11a	*128*	6	40(xM)
UWB	128	4	1580
BPL	512 or1024	18	3

Table1: FFT requirements of OFDM and MxM MIMO OFDM standards

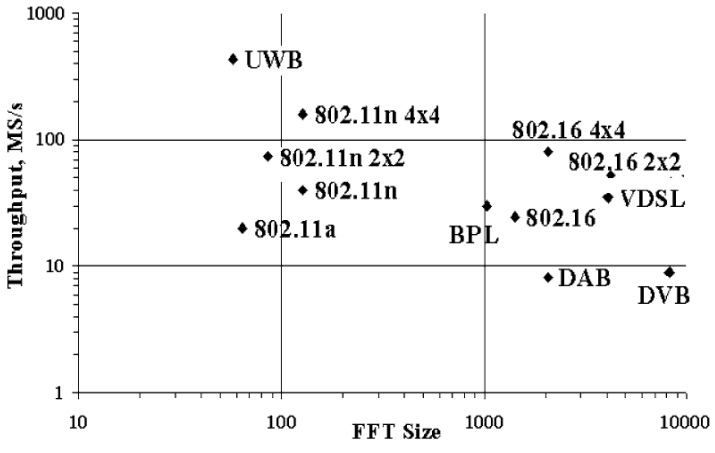

Figure2: FFT throughput, size for different OFDM and MIMO-OFDM transceivers

Based on single input single output (SISO), the throughput is increased M times in MxM MIMO-OFDM standards. These

requirements are mainly for mobile terminals. For high throughput application the massively parallel architecture for FFT is suitable one. Now we see the different a framework in FFT for the OFDM system.

III. FULLY PARALLEL FRAMEWORK:

This approach allows a memory free design and has a very high throughput. This is right choice for choosing FPGA than ASIC design, because the clock frequency is lower than the ASIC design. The parallel design has a hoc customization for controlling the width of the data flow stage by stage. The logic synthesis tool optimizes the all multiplication in the algorithm which is turned to multiplication by constant factor. The fixed point representation of real and imaginary or both multiplicands is reduces to trivial values such as zero or ± power levels, these are costless in implementation level

VLSI framework: Every stage of the parallel frame work of the FFT is collected of the butterfly blocks. It has the N complex multiplication factor by twiddle factor. The twiddle factor takes the different constant values over the stages of FFT parallel framework for the time sharing frameworks. For increasing the speed of elaboration and reducing the complexity in parallel booth architecture, the multipliers not need any particular framework. it done by the lifting approach. It can be described as following, instead of four multiplications and two additions it require only three multiplications and three additions. This approach reduces the complexity but increase the delay of critical path in design. So this is only suitable for low complexity and low throughput application.

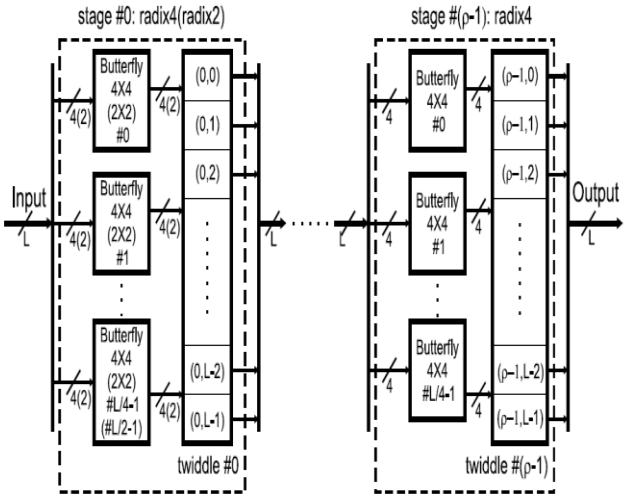

Figure 3: FFT radix framework

IV. BASICS OF UWB (ULTRA WIDE BAND):

The UWB technology transmits the information over a large band width. OFDM uses the UWB bands for transmitting the information in high speed. The N point parallel FFT design computes the N complex samples per clock cycle. So it produce the throughput as a few M samples/s. for example we take the 128 –point parallel FFT, it computes the 128 complex samples per the clock cycle, so it can produce the throughput of 1586 Msamples/s with clock frequency of 12.37 MHZ. The UWB signal quantize only 4-6 bits, it is very difficult in VLSI design. For quantizing the 5 bits with signal to quantized noise ratio (SQNR) is 26db, we round up and saturate the output of the transformer after every butterfly and lifting multiplication. If we increase the twiddle factor quantization factor, we get maximum SQNR rate.

The twiddle factors are quantized up to 6 bits, and it has the maximum SQNR rate of 27db.it is a free growing data flow process. The parallel FFT adopts the lifting model approach. The lifting co efficient is L_1 andL_2, it can be quantized up to 6 bits. After every multiplication it discarded as quantized bits -1 bits.

V. CASCADE FRAMEWORK:

It is an alternative design of parallel FFT framework. It used in a many multimedia and communication because it provides low complexity and high speed and more flexibility. We take the cascade of radix-4 butterfly, this support stream oriented data stream.

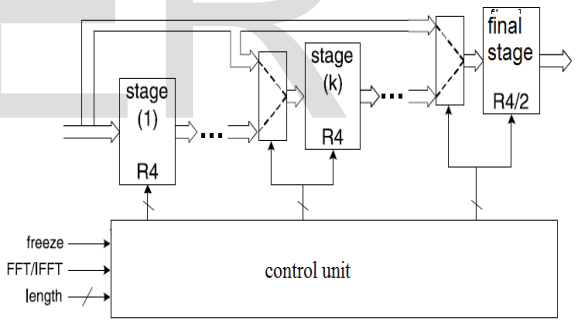

Figure4: programmable cascade framework

The above figure shows the programmable cascade framework of the FFT core. The size of the FFT/IFFT can be configured by the number of the stages in the cascade framework at the run time. During the switching between the FFT and IFFT computational the freeze and flush signals are control the internal pipeline. Here we use the memory banks in data sequence model for storing the data. We use the RAM and ROM memory, the RAM for data and ROM for twiddle coefficient. In FFT the ROM stores the real and imaginary parts same as in IFFT it stores the conjugate of the twiddle factor. The top level data path of the cascade framework is fully parametric in terms of the maximum size of the FFT, number of the radix stages, and world length of the I/O and twiddle coefficient of the internal system data path. Each radix supports the different types of the machine arithmetic, which is fixed point arithmetic and blocked point

arithmetic and also the convergent block floating point arithmetic. The complex multiplier has three multipliers and six adders. So the cascade approach is more complex in the parallel framework. Every radix stage is including the multiple butterfly architecture in parallel framework. In cascade approach is use the single butter fly per stage. So the length of the FFT is considered by the number of butterflies and the relevant hardware complexity. From this case the cascade is minimized than the parallel approach. The buffering capabilities are embedded with the data path. Based on the small memory banks the data sequence is designed and managed. The UWB and MIMO systems with large number of channels and a cascade framework ,which required a clock. The cascade approach is only suitable for the mid range application such as DVB, WLAN, DAB, DSL.WMAN.

VI. IN –PLACE VARIABLE LENGTH FFT:

Here we seen about the reconfigure FFT framework, it is suitable for the 4x4 MIMO OFDM wireless systems that process up to 4 data streams that is varied in length of the symbol. That is varied from 128-2046.here our proposed prototype uses a in-place framework, it produce assorted FFT output. The input element is stored in the register banks. Index of each LSB element is stored in the register bank. At the output of every butterfly stage the following stage is performed. The transformation couple stage is formed by the x_s ,x_r element at the i^th stage, the elements are changed only at the i^th bit.

If the (j+1) stage of the elements x_s and x_r is 1, the results are change its memory locations. The output elements are stored with the 0, . . . , $^N/_2 - 1$ indices in the register bank B_i,0. If the value is increased the output is stored in the B_i,1 register bank. And also see the butterfly architecture, it has two inputs, that is I_R and I_S and the output is O_R and O_S.

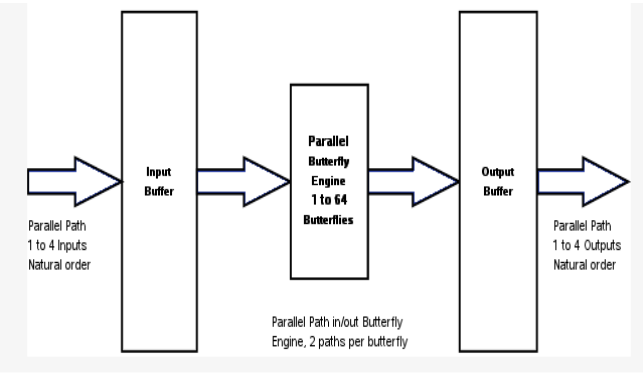

Figure 5: In-place variable length framework

It has dual memory banks, twiddle bank, data and address generation bank.

VII. SUMMARY OF FFT:

By using in-place technique with radix-2 factorization, the engine computes FFT-DIT (decimation in time) algorithms. It made of 16 butterflies .32 register banks and interconnection network to make a group of processor as 2/4/8/16. At a run time the FFT can be computed as a 32/64/128 complex point. At a run time every processor can be re configured. Depending up on the length of the 4FFT the reconfiguration and grouping of the processors can be determined. Furthermore we include the input buffer and two modes for scheduling. For using one stream of data with symbol length is greater than are equal to 1024, we use first mode. So here each processor use 128 point FFT .Remaining cases switch by a mode 2.In first mode the input buffer used to collect the symbols which have a same length. The collection of data the computes to the processor engine in round robin model.

In second model the symbol from each stream is assigned to devoted group of four processors. The streams are processed in parallel streams. Here our proposed model uses in-place technique for producing the variety output of the FFT. Every radix-2 butterflies have 2 inputs and 2 outputs and also have the dual port memory banks, FFT control, inter connection, address and data generation and twiddle generation. Taking the 128 point processor, the FFT control adds 10 bits up counter to hold 1024 pairs of data and 4 bits down counter to hold the stages of the FFT

VIII. RESULT FOR COMPARING THE FRAMEWORK OF FFT:

Here we produce a result by comparing the three frame work of the FFT with state of art of the FFT-VLSI prototyping. We can compare the throughput and numerical accuracy of the three proposed frame works. First we compare the cascade framework with state of art of FFT, for DVB-T/H application. The gate complexity is 37 and memory complexity for RAM 21975, and for ROM 8180. It is automatic IP generator, have a clock frequency about 9MHZ, the SQNR rate is greater than 40db.

The parallel architecture, the clock frequency is 132MHZ with delay of 0, 90, 180 and 270.the delay degrees are generated by digital clock management part. This framework can be compared with UWB FFT core which is proposed by sherrat el al. by fitting with FPGA, the UWB FFT requires 5000 slices of vertix4 device. But our proposed full parallel framework requires only 2000 slices of vertex4 devices. By this we achieve the throughput is 7 Gsamples/s with clock frequency rate of 55MHZ.

Consider the final frame work, in-place, reconfigurable framework, the target implementation is 10 bit FFT on vertex FPGA. The FFT core contains 8610 slices, 80 ram, 60 DSP blocks. Its operating frequency is 34MHZ and SQNR is 56db. Now we are compare the propose frame work with each other. The first two frameworks have a fixed input length and the third one has a variable input length. The high expensive parallel and cascade frameworks offered

the increased input data stream. And the high expensive hardware of the fully parallel offers the high throughput rate. The cascade offers the high throughput rate with low hardware resources compared with in-place variable reconfigurable framework.

For easy comparison we have taken three cases. In first case we take 5 bits I/O and 128 point processor, the fully parallel occupies the 2274 slices and 7Gsamples/s of throughput. And the cascade has 32 Msamples/s and 6226 slices. In case-2 we have taken 1024 points and 8 bit I/O processor. Based on this the fully parallel has 13425 slices and 50 Gsamples/s. and the cascade has 12405 slices and 132 Msamples/s. the third case we have taken variable length 10 bit processor, in this cases we only taken in-place reconfigurable framework it has 100 Msamples/s of throughput and 1871 slice. From this, the cascade framework is suitable for DAB and DVB-T/H, xDSL and BPL telecom standards. The in-place variable reconfigurable framework supports the 802.16d/e and 802.11n standards. And the parallel framework is suitable for the UWB standards.

Conclusion:

Our aim is to prototyping the different FFT/IFFT frameworks for multicarrier OFDM based telecom application. In this paper we proposed three different frameworks for the aimed application. There are cascades, parallel and in-place variable length reconfigurable frameworks. From this work we suggest the fully parallel framework is provide a best fine technique for the UWB when all the channels are used, because the fully parallel framework is offer high throughput rate, 1tens of Gsamples/s. the cascade framework offer a well-organized pipeline for SISO systems and have a large FFT input length. And finally we combine the reconfiguration and in-place technique; we produce a low cost system for MIMO with variable input size of FFT.

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